CBCS SCHEME

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21CS33

Third Semester B.E. Degree Examination, Dec.2023/Jan.2024
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is BiaSing? List the types of BiaSing and discuss fixed bias. **(06 Marks)**

b. Describe the working of Schmitt trigger circuit (non inverting) with transfer characteristics. **(08 Marks)**

c. Explain First Order Low Pass Filter with Mathematical Analysis. **(06 Marks)**

OR

2 a. Discuss Regulated power supply with block diagram. **(06 Marks)**

b. With neat sketch, explain successive approximation ADC method. **(08 Marks)**

c. With the help of a neat diagram, explain the working principle of relaxation oscillator. **(06 Marks)**

Module-2

3 a. Reduce the following function using K-map technique and implement the expression with Basic gates :

$f(a,b,c,d) = \sum m(0, 1, 6, 8, 9, 11) + \sum d(3, 7, 14, 15)$ **(10 Marks)**

b. What are Prime Implicants? Find all the prime implicants and simplified expression for the function using Q-M method,

$f(a,b,c,d) = \sum m(0, 2, 3, 4, 8, 10, 12, 13, 14) + d(11, 15)$ **(10 Marks)**

OR

4 a. Simplify the following POS expression using K-map and implement using Basic gates,

$f(a,b,c,d) = \Pi M(0, 1, 3, 4, 5, 7, 11, 12, 13, 14, 15)$ **(08 Marks)**

b. Obtain the simplified expression using EVM method for the given function,

$f(a,b,c,d) = \sum m(0, 1, 5, 13, 14, 15) + dC(8, 9, 10, 11)$ **(06 Marks)**

c. With example, explain Petrick's method. **(06 Marks)**

Module-3

5 a. Implement the following function using 8 : 1 multiplexer,

$F(a,b,c,d) = \sum m(0, 1, 5, 6, 8, 10, 12, 15)$ **(07 Marks)**

b. Implement 7-segment decoder using PLA. **(08 Marks)**

c. Discuss Four kinds of three state buffers. **(05 Marks)**

OR

6 a. Implement Full Adder using 3 : 8 Decoder. **(07 Marks)**

b. Design Hexadecimal to ASCII code converter using suitable ROM. Give the connection diagram of ROM. **(08 Marks)**

c. Explain static 1 Hazard with its recover method. **(05 Marks)**

Module-4

7 a. Explain the structure of VHDL program. Write VHDL code of JK Flip Flop. (08 Marks)
b. Derive characteristic equation of JK, D, D, SR flip flops. (08 Marks)
c. What is T-FF? Give the implementation circuit. (04 Marks)

OR

8 a. Explain Master Slave JK FF with neat diagram, Truth table and timing diagram. (08 Marks)
b. What are the three different models of writing module body in VHDL. Give VHDL code of 4 : 1 multiplexer using conditional assign statement. (08 Marks)
c. Give excitation table of JK and SR FF. (04 Marks)

Module-5

9 a. With a neat diagram, explain n-bit parallel Adder with Accumulators (10 Marks)
b. Design Mod-8 Counter using JK Flip flop. (10 Marks)

OR

10 a. With neat diagram, explain SISO register. (10 Marks)
b. Design a synchronous counter for the given sequence.
$0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0 \rightarrow 4$ (10 Marks)

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